REMARKS

This is in full and timely response to the non-final Office Action mailed on May 24, 2002, Reexamination in light of the following remarks is respectfully requested.

Claims 13-37 are pending in this application, with claims 13, 18, 22, 26, 30 and 34 being independent. No new matter has been added.

Drawings

Figures 12A, 12B, 14A, 14B, 14C, 14D, 14E, 14F, 15A-1, 15A-2, 15B, 15C-1, 15C-2 have been amended as requested by the Examiner. Withdrawal of the objection to the drawings is respectfully requested.

Abstract

The Abstract has been amended as requested by the Examiner. Withdrawal of the objection to the Abstract is respectfully requested.

Rejections Under 35 U.S.C. §102 and §103

In response, while not conceding the propriety of this rejection, and in order to further the prosecution of the

application, claims 1-12 have been canceled, rendering this rejection moot. Withdrawal of this rejection is respectfully requested.

Newly added claims

Within newly added claims 13-25, a sampling signal has a plurality of pulses during each cycle of the clock signal. A plurality of logic levels is generated during each cycle of the clock signal. A logic level of the plurality of logic levels is the signal level of the received signal when sampled by a pulse. The decoder decodes the plurality of logic levels to generate the received data.

U.S. Patent No. 5,850,187 issued on Carrender et al. (Carrender) arguably teaches an integrated electronic tag reader and wireless communication link. Nevertheless, Carrender fails to disclose, teach or suggest a sampling signal having a plurality of pulses during each cycle of the clock signal.

U.S. Patent No. 5,602,879 issued to Wada arguably teaches a clock recovering circuit. Figures 8 and 26 of Wada arguably depict a plurality of sampling points. Wada arguably teaches using the sampling points to determine the correlation between

data at adjacent pairs of sampling points (column 6, line 64 to column 7, line 1). The sampling points of Wada are arguably used to produce a timing clock (column 7, lines 37-55).

However, Wada fails to disclose, teach or suggest logic level of the plurality of logic levels being the signal level of the received signal when sampled by a pulse and fails to disclose, teach or suggest the decoder decoding the plurality of logic levels to generate the received data, as claimed.

Within newly added claims 26-37, a correlation value detection circuit compares the phase of the clock signal to the phase of the received signal to generate a correlation value signal. The correlation value signal trends in a first direction when the clock signal is in phase with the received signal and trends in a direction opposite to the first direction when the clock signal is out of phase with the received signal.

These features are not found within Carrender and Wada, either individually or as a whole. Allowance of the claims is respectfully requested.

Conclusion

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance. Accordingly, favorable reexamination and reconsideration of the application in light of the amendments and remarks is courteously solicited.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753 or the undersigned attorney at the below-listed number.

Respectfully submitted,

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